differential pair for the IC by employing both the first sinusoidal signal and the second sinusoidal signal to form the clock signal".

It is noted that the circuitry disclosed in the Wissell et al. reference does not employ both sinusoidal signals received as inputs to the receiver chip shown in FIG. 3 to generate either of the digital clock signals output from the receiver chip of FIG. 3. Specifically, the "digital SIN clock signal" is formed only from the "SIN" sinusoidal input, and the "digital COS clock signal" is generated only from the "COS" input sinusoidal signal. Accordingly, it is submitted that claim 1 is now patentably distinguished from Wissell et al., by virtue of its recitation of employing both first and second sinusoidal signals to form a clock signal.

The other rejected independent claims, which are claims 8, 13 and 22, have been amended in substantially the same fashion as claim 1, and are submitted as patentable over Wissell et al. on the same basis as claim 1. In addition, the rejected dependent claims 2-7, 9-12, 14-21 and 23-30 are submitted as patentable on at least the same basis of their respective parent independent claims. Regarding the Examiner's statement that "it is inherent that peak-to-peak amplitude of the sinusoidal signal is less than the peak-to-peak amplitude of the local clock signals because the local clock signals are achieved by amplifying the sinusoidal clock signals," the Examiner is respectfully referred to column 5, line 59 - column 6, line 13 of the Wissell et al. reference which describe the use of step down transformers within the receiver circuits as well as amplifiers, filters and buffers.

New claims 31-34 are now presented to more completely cover the invention.

Claim 31 is directed to a "method of generating a clock signal on an integrated circuit (IC)". Claim 31 recites "generating a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal" and "generating a clock signal from the differential pair for the IC by subtracting the first sinusoidal signal from the second sinusoidal signal".

It is noted that neither the Wissell et al. reference nor the other prior art of record teaches or suggests generating a clock signal by subtracting a first sinusoidal signal from a second sinusoidal signal. Accordingly, it is submitted that claim 31 is patentable over the prior art of record.

The other three newly-presented claims, namely claims 32-34, are all in independent form. Each of these three claims, like claim 31, recites in substance the feature of generating a clock signal by subtracting a first sinusoidal signal from a second sinusoidal signal. Accordingly, claims 32-34 are submitted as patentable on at least the same basis as claim 31.

In view of the foregoing, it is submitted that all of the pending claims are in condition for allowance, and passage to issue is respectfully solicited.

In addition to the requisite fee of $740.00 for filing the Request for Continued Examination, an additional fee of $408.00 is included to cover four independent claims and four total claims in excess of those for which payment had previously been made. Applicants do not believe any other fees are due regarding this amendment. If any additional fees are required, however, please charge Deposit

Account No. 04-1696. Applicants encourage the Examiner to telephone Applicants' attorney to discuss the amendment should any issues remain.

Respectfully submitted,

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VERSION MARKED TO SHOW CHANGES

In the Claims:

Claims 1, 8, 11, 13, 22 and 30 have been amended as follows:

1. (Amended) A method of generating a clock signal on an integrated circuit (IC), the method comprising the steps of:

generating a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal; and

generating a clock signal from the differential pair for the IC by employing both the first sinusoidal signal and the second sinusoidal signal to form the clock signal.

8. (Amended) A method of driving a clock tree on an integrated circuit (IC), the method comprising the [step] steps of:

providing an IC having a clock tree; [and]

distributing a clock signal in the form of a differential sinusoidal signal pair in a portion of the clock tree, the differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal; and

generating a local clock signal from the differential pair by employing both the first sinusoidal signal and the second sinusoidal signal to form the local clock signal.

11. (Amended) The method of claim 8, [further comprising converting] wherein generating the [differential sinusoidal

signal pair to a] local clock signal [by] includes using a differential amplifier.

13. (Twice amended) A clock circuit for an IC, comprising:

a generating circuit adapted to generate a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal;

a distribution circuit coupled to the generating circuit and adapted to distribute the differential sinusoidal signal pair on the IC; and

a plurality of clock receiver circuits coupled to the distribution circuit and adapted to convert the differential sinusoidal signal pair into respective local clock signals by employing both the first sinusoidal signal and the second sinusoidal signal to form each local clock signal.

22. (Amended) Apparatus for generating and distributing a clock signal, comprising:

means for generating a differential sinusoidal signal pair comprising a first sinusoidal signal and a second sinusoidal signal;

means for distributing the generated differential sinusoidal signal pair; and

means for receiving the distributed differential sinusoidal signal pair and [converting the received differential sinusoidal pair into] generating a local clock signal from the received differential sinusoidal signal pair by employing both the first sinusoidal signal and the second sinusoidal signal to form the local clock signal.

30. (Amended) The apparatus of claim 22, wherein the means for receiving and [converting] generating includes a differential amplifier.